Evaluation of Electrical Stress Effect on Class *F* Power Amplifier by Simulation

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Abstract

A class *F* power amplifier has been designed using TSMC 0.18 μm CMOS mixed-signal RF technology at 5.8 GHz. The PA's output power and power-added efficiency have been evaluated using the ADS simulation. Physical insight of transistor operation in the RF circuit environment has been examined using the Sentaurus mixed-mode device and circuit simulation. The transient drain-source voltage waveform indicates that the output stage transistor is under much higher voltage stress than that of the input stage transistor. The hot electron effect and device self-heating degrade the output power and power-added efficiency of the power amplifier, especially when both the input transistor and output transistor suffer high impact ionization rates and lattice heating.

Keywords

Class F; Hot Electron; Oxide Stress; Power Amplifier; Reliability

Introduction

The advance in CMOS technology for high frequency applications has made it a natural choice for integrated, low cost RF power amplifiers (PAs) for wireless communications ICs. Depending on its applications, the power transistor can be used as a current source (class A, B, and C mode) or a switch (class D, E, and F mode). Switching-type amplifiers achieve high power efficiency [1] and are desirable for portable communication systems such as cell phones, global position systems, and wireless local area networks. The tradeoff between linearity and efficiency in power amplifiers has been investstigated extensively. To linearly amplify the modulated signals, the PAs typically operate in a back-off power region at the expense of efficiency. However, polar modulation transmitter achitecture [2,3], where a phase modulated signal with constant envelope is amplified by a non-linear (switching type) PA, has the potential to enhance the efficiency while achieving high linearity.

Due to aggressive scaling in device dimensions for improving speed and functionality, CMOS transistors in the nanometer regime continue to endure major reliability issues such as channel hot electron degradation [4,5] and gate oxide breakdown [6,7]. In the past 10 years, numerous papers on the stress effect on digital and RF circuits have been published [8-12]. For example, the gate oxide stress decreases the static noise margin of 6-transistor SRAM cells [8]. Hot electron increases the noise figure of the low-noise amplifier [9-11], and the phase noise of the voltage-controlled oscillator [12, 13].

In this work, a class *F* power amplifier is designed. Its RF performances before and after layout are analyzed. Sec. 2 describes the design of the class *F* power amplifier. Sec. 3 presents the Cadence layout and posts layout simulation results. Sec. 4 illustrates the physical insight of the device behavior in the class *F* PA operation environment. Finally, conclusions are given in Sec. 5.

Design of a Class-F PA

The Class *F RF* power amplifiers utilize multiple harmonic resonators in the output network to shape the drain-source voltage. The drain current flows when the drain-source voltage is low, and the drain-source voltage is high where the drain current is zero. This reduces the transistor switching loss and increases the drain efficiency of the class *F PA*. In class *F* amplifiers with odd harmonics, the drain-source voltage contains only odd harmonics and the drain current contains only even harmonics. Thus, the input impedance of the load network represents an open circuit at odd harmonics and a short circuit at even harmonics. The V_{DS} of class *F PA* with odd harmonics can be written as

$$V_{DS} = V_{DD} - V_m \cos(\omega_0 t) + \sum_{n=3,5,7,\ldots}^{\infty} V_{mn} \cos(n\omega_0 t) \quad (1)$$

where V_{DD} is the supply voltage, V_m is the fundamental component of drain voltage, V_{mn} is the amplitude of n-

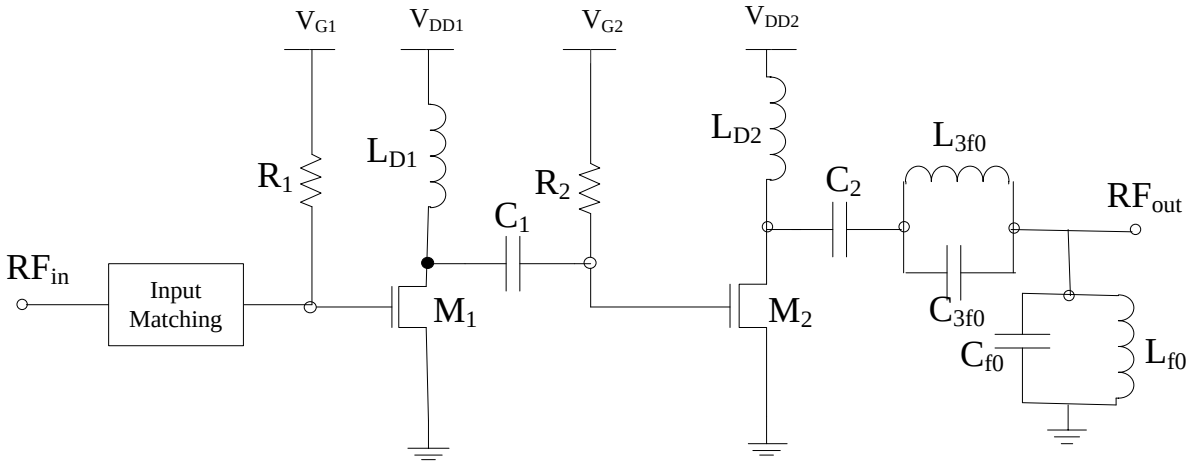


Fig. 1 Schematic of class F power amplifier

th harmonic of V_{DS}, and ω_0 is the angular frequency at the operating point.

The drain current i_D is given by

$$i_{DS} = I_{DD} + I_m \cos(\omega_0 t) + \sum_{n=2,4,6,...}^{\infty} I_{mn} \cos(n\omega_0 t) \quad (2)$$

where I_{DD} is the *DC* current from V_{DD}, I_m is the fundamental component of drain current, I_{mn} is the amplitude of n-th harmonic of i_{DS}. No real power is generated at harmonics because there is neither no currentnor no voltage presented at each harmonic frequency. In class *F* amplifiers with even harmonics, on the other hand, the drain-source voltage contains only even harmonics and the drain current contains only odd harmonics.

In this work, the *PA* is designed with third hamonic peaking. The detail of class *F PA* design can be referred to [1]. The load network consists of a parallel *LC* resonant circuit tuned to the operating frequency f_0 and a parallel resonant circuit tuned to the third harmonic $3f_0$. The two resonant circuits are connected in series. The *ac* power is delivered to the load resistor. Fig. 1 shows the schematic view of the *PA* with a class-*F* output stage. The output of the input stage transistor is connected to the gate of the output stage transistor by a coupling capacitor C_1. The circuit is tuned and simulated using ADS software [14].

Using TSMC 0.18 μm mixed-signal CMOS technology library, the class F power amplifier shown in Fig. 1 is evaluated in ADS. Multi-finger n-channel transistors are used in the input stage and output stage transistors. The input stage transistor M1 has a channel length of 0.18 μm and channel width of 256 μm. The output stage transistor M2 has a channel length of 0.18 μm and channel width of 512 μm. The DC supply voltages V_{DD1} and V_{DD2} are equal to 2.4 V. The gate DC voltages of M1 and M2 are at 0.4 V and 0.5 V, respectively. Biasing resistors R_1 = 10 kΩ and R_2 = 1 kΩ. The inductor and capacitor values used in this design are L_{D1} = 1.95 nH, L_{D2} = 2.06 nH, L_{3f0} = 0.31 nH, L_{f0} = 1.04 nH, C_{3f0} = 277.9 fF, C_{f0} = 748.6 fF, C_1= 1 pF, and C_2= 2 pF. The inductor quality factor Q is accounted for in TSMC spiral inductor models. The simulated results of output power and power-added efficiency are presented in Sec. 3.

Cadence Layout and Post-layout Simulation

The class F power amplifier has been laid out using Cadence Virtuoso software, followed by Calibre DRC for design rule checking and LVS for layout versus schematic verification. A silicon chip layout of 726×950 μm² is displayed in Fig. 2. In this figure spiral inductors, capacitors, transistors, GSG RF input and output pads, biasing and supply voltage DC pads are shown. The layout (interconnection) parasitic effects are extracted using ADS Momentum EM simulation to generate s-parameters. These s-parameters implicitly account for interconnect resistive, capacitive, and inductive behaviors. The extracted interconnect parasitic effects (s-parameter boxes) are then added to the original ADS circuit simulation for post-layout simulation. The post-layout simulation results are shown in Figs. 3 and 4. The layout parasitic effect decreases the output power and power-added efficiency of the amplifier, as expected. Parasitic resistance introduces additional power loss in the circuit which reduces the power efficiency. Layout

interconnections are very important for CMOS RFIC parasitic effects [15]. To reduce layout parasitic effects, we adjust inductors, capacitors, and transistors location and orientation in our design.

The simulated output current and voltage versus time, output power and power-added efficiency versus input power are as shown in Figs. 3 and 4, respectively. In Fig. 4 the line with triangles represents the pre-layout simulation results and the line with squares represents the post-layout simulation results. As seen in Fig. 4 the output power increases with input power and reaches saturated output power at about 17.5 dBm. The post layout parasitics decrease the output power at a given input power. The power-added efficiency (≡ (RF output power - RF input power)/total DC power dissipation) increases with input power, reaches its peak value, and then decreases with input power. The power-added efficiency starts to decrease after reaching its peak because of the gain reaching a compression point, resulting in the output power no longer increasing. The maximum power-added efficiency approaches 32%, and drops to 29.5% after post-layout simulation. Note that the power-added efficiency is lower than the drain efficiency because of additional power dissipation in the input stage.

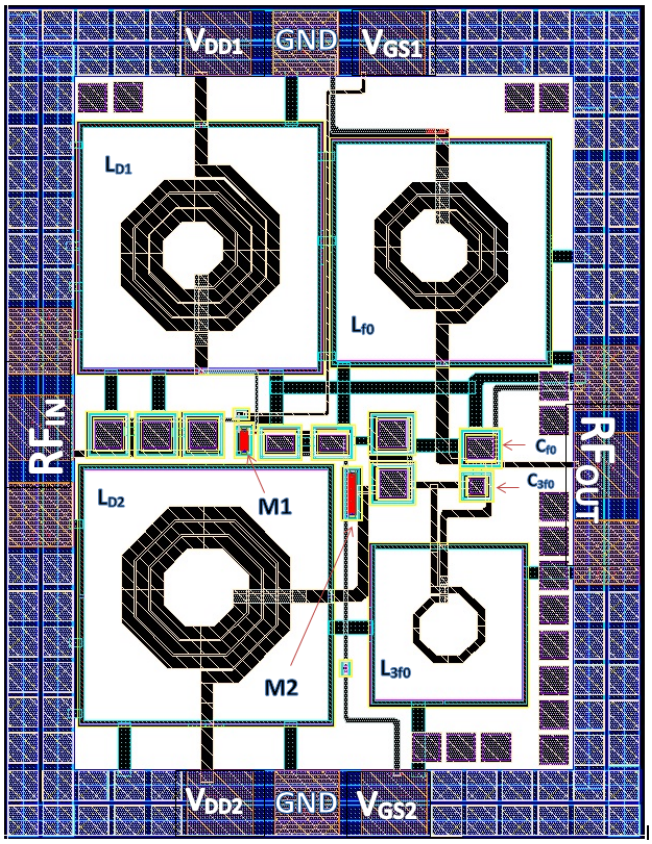


FIG. 2 LAYOUT VIEW OF THE CLASS F POWER AMPLIFIER

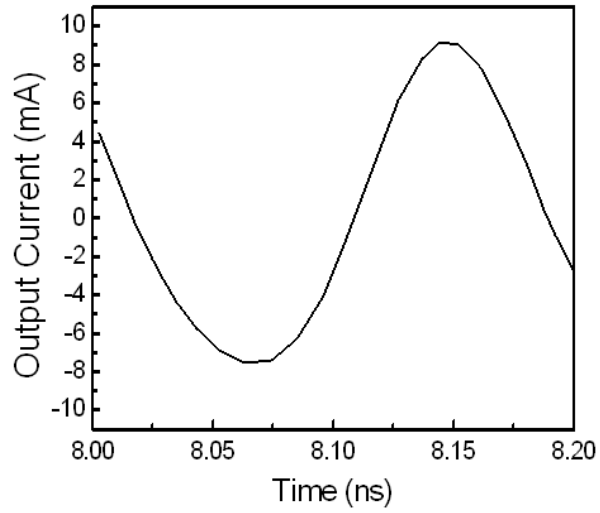


FIG. 3(A) OUTPUT CURRENT VERSUS TIME

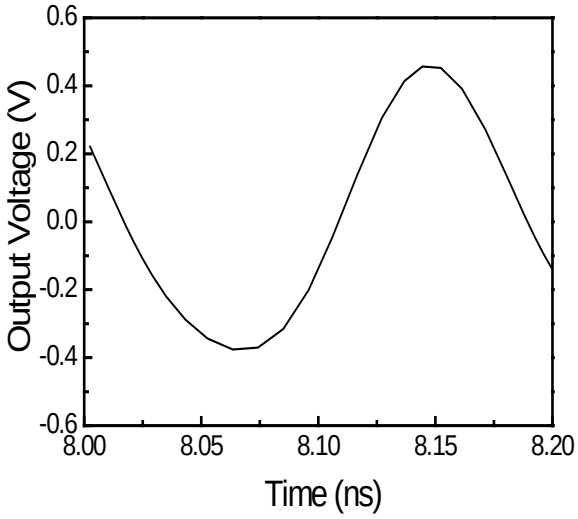


FIG. 3(B) OUTPUT VOLTAGE VERSUS TIME

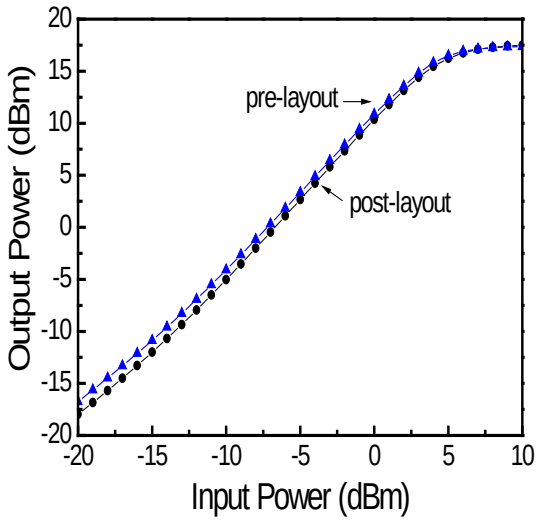


FIG. 4(A) OUTPUT POWER AND POWER GAIN VERSUS INPUT POWER

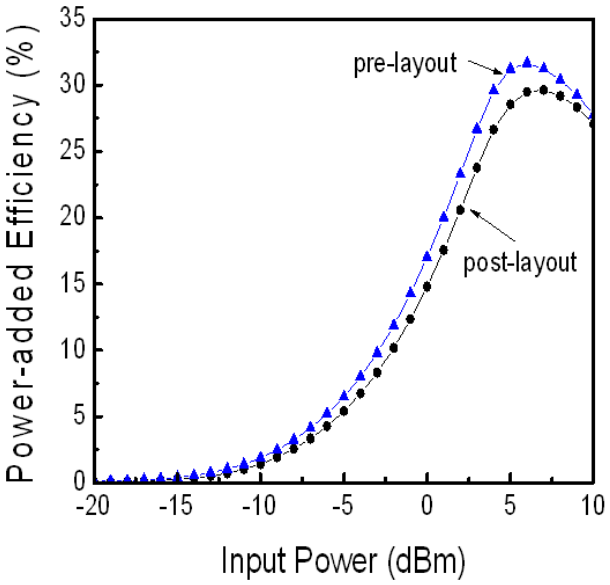


FIG. 4 (B) POWER-ADDED EFFICIENCY VERSUS INPUT POWER

Physical Insight Using Mixed-Mode Device and Circuit Simulation

To evaluate the physical insight of hot electron effect in RF operation, the mixed-mode simulation of Sentaurus TCAD software is used [16]. The mixed-mode device and circuit simulation allow one to evaluate the device physical insight under the real circuit opreation condition. In Sentaurus simulation, physical equations such as Poisson's and continuity equations for drift-diffusion transport are implemented. The Shockley-Read-Hall carrier recombination, Auger recombination, and impact ionization models are also used. The impact ionization van Overstraetende Man model [17] assumes the impact ionization coefficient to be a function of the local field. To account for lattice heating, Thermodynamic, Thermode, RecGenHeat, and AnalyticTEP models in Sentaurus are used. The thermodynamic model extends the drift-diffusion approach to account for electrothermal effects. A Thermode is a boundary where the Dirichlet boundary condition is set for the lattice. RecGenHeat includes generation-recombination heat sources. AnalyticTEP gives analytical expression for thermoelectric power. The ambinet temperature is at 300 K. Figs. 5 and 6 show the gate-source voltage and drain-source voltage of the input transistor M1 and the output transistor M2 from Sentaurus simulation. It is clear from Figs. 5 and 6 that the output transistor has much larger V_{GS} and V_{DS} swings than those of the input transistor. When the gate-source voltage is above the threshold voltage and the drain-source voltage is very high, the transistor is under high electric field stress. Sufficient high field may trigger device avalanche and hot carrier injection.

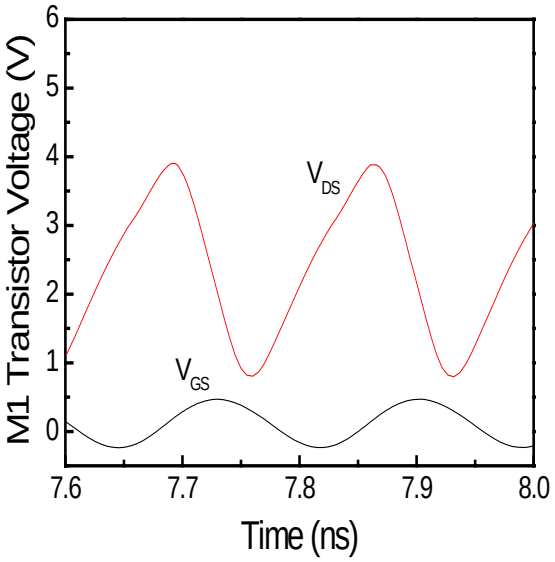


FIG. 5 DRAIN-SOURCE AND GATE-SOURCE VOLTAGE OF THE INPUT TRANSISTOR M1

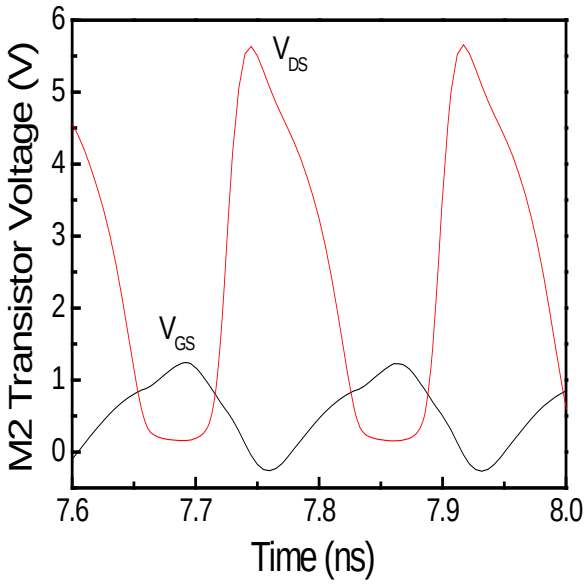


FIG. 6 DRAIN-SOURCE AND GATE-SOURCE VOLTAGE OF THE OUTPUT TRANSISTOR M2

Fig. 7 shows impact ionization rates for the input and output transistor transistors of the PA at high V_{DS}. The supply voltage in Sentarus simulation is set at V_{DD} = 3.3 V. As seen in Fig. 7 the I.I. rates at the peak of output voltage waveform from M2 (left plot) are much higher than those in M1 (right plot). High impact ionization rates (2×10^{30} /cm^3/s) at the drain of M2 transistor suggest large hot electron injection into the

gate of the M2 near the drain edge. Hot electron effects result in the MOS transistor performance degradation [18]. Fig. 8 shows the lattice temperature of M1 and M2. The maximum lattice temperature at the drain of M2 increases to about 320 K, while the lattice temperature of M1 is virtually the same from source to drain. The current density in M2 is higher than that in M1 due to larger gate-source voltage and drain-source voltage simultaneously (data not shown here). High curernt density and high drain voltage produce self-heating and high lattice temperature near the drain edge.

From the reliability point of view, the output stage transistor of the class F power amplifier is more vulnerable to channel hot electron effect and gate oxide stress. It is clear from Fig. 6 that the peak drain-gate voltage of the second stage transistor is above 5.6 V due to larger V_{DS} and V_{GS} which provides high voltage stress between the drain and gate oxide. For example, the electric field of a 4-nm oxide thickness at 5.6 V voltage stress can approach 14 MV/cm, a precursor for gate-drain oxide breakdown. Note that the drain stress voltage can further increase when the supply voltage V_{DD} increases.

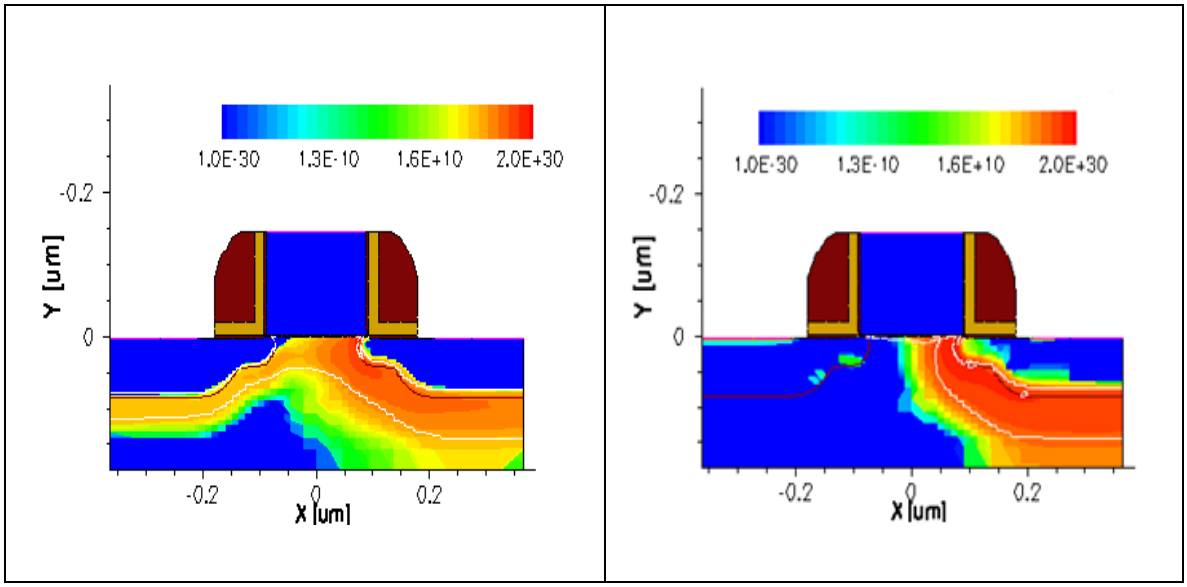


FIG. 7 IMPACT IONIZATION RATES OF THE INPUT STAGE (LEFT PLOT) AND OUTPUT STAGE (RIGHT PLOT) TRANSISTORS

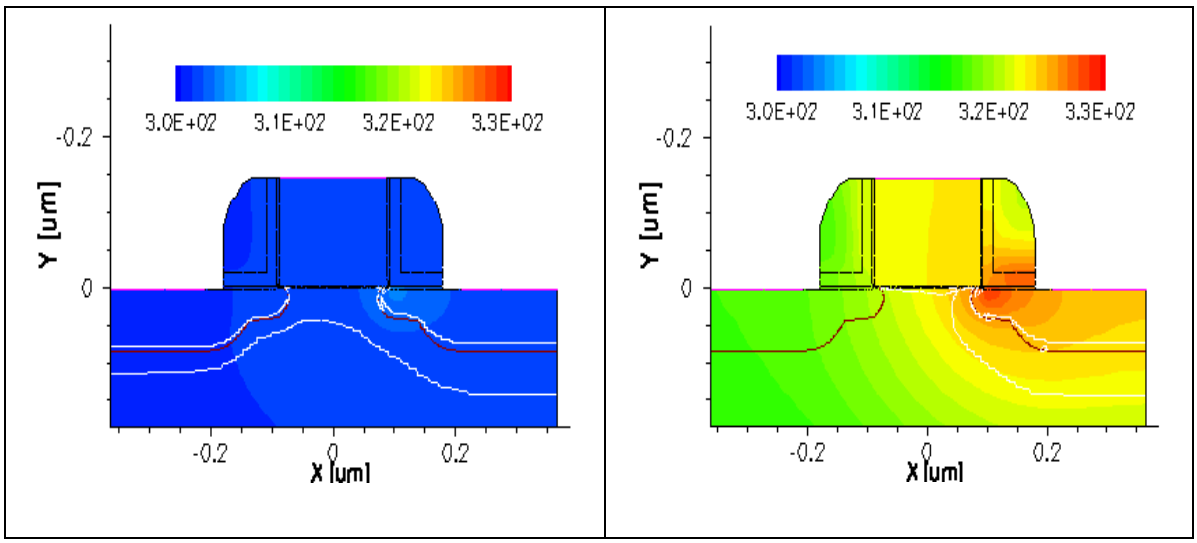


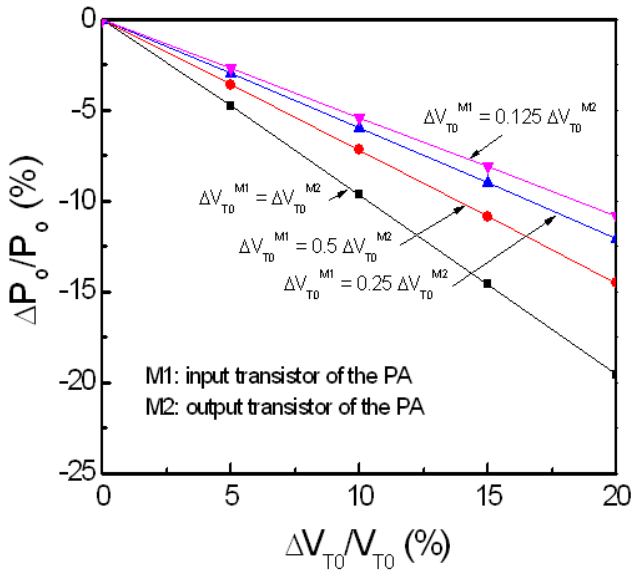
FIG. 8 LATTICE TEMPERATURE OF THE INPUT STAGE (LEFT PLOT) AND OUTPUT STAGE (RIGHT PLOT) TRANSISTORS

The oxide under high voltage stress may experience some kind of soft breakdown before hard breakdown [19]. Soft breakdown increases the gate leakage current noise due to formulation of random defects and conducting path within the oxide [20]. Soft breakdown effect may be modeled using nonlinear current sources [21, 22], while the hard breakdown can be realized by using breakdown resistances [23]. In general, oxide breakdown decreases the output power and power efficiency of power amplifiers [24].

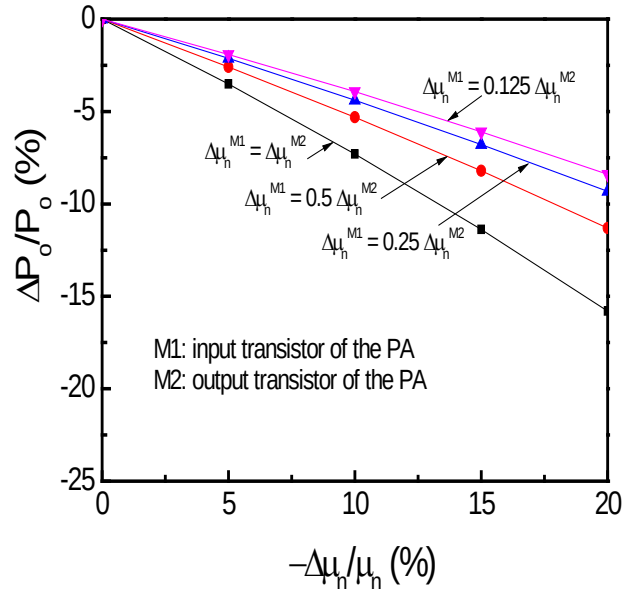
Impact of Hot Electron Effect Stress and Self-Heating Effect on Class F PA

Hot electron injection originates from energetic electrons or holes in the channel entering oxide layer to produce oxide trap charge and interface states, which in turn increases the transistor threshold voltage and decreases the effective channel electron mobility. The output power and power-added efficiency versus threshold voltage shift and mobility degradation are depicted in Figs. 9 and 10, respectively. In general, the threshold voltage shift accumulates over time ($\Delta V_T \propto t^n$). To account for different degrees of hot electron stress effects on M1 and M2 over a period of time, the shift of threshold voltage in M1 is modeled differently than that in M2. For example, ΔV_{T0} in M1 could be set to 1/8, ¼, ½, and $1\times\Delta V_{T0}$ of M2. As seen in Fig. 9(a) the largest output power degradation occurs when $\Delta V_{T0}^{M1} = \Delta V_{T0}^{M2}$. This is because the output of the first stage transistor M1 drives the second stage transistor M2 for output power. When the input transistor's driving current drops, the overall output power of the PA decreases. Similar characteristics are observed for the output power versus electron mobility shift. The output power decreases when the electron mobility decreases. The worst case of degradation occurs when $\Delta\mu_n^{M1} = \Delta\mu_n^{M2}$ as shown in Fig. 9(b).

Furthermore, the normalized power-added efficiency versus normalized threshold voltage shift and mobility degradation has been examined. The simulation results are shown in Fig. 10. The power-added efficiency decreases with the increase in threshold voltage and the decrease in electron mobility. Again, the worst case of degradation occurs when $\Delta V_{T0}^{M1} = \Delta V_{T0}^{M2}$ and $\Delta\mu_n^{M1} = \Delta\mu_n^{M2}$. To reduce hot electron degradation effects on power amplifier performance, the cascode transistor topology may be used to reduce electron field on the drain edge of MOS transistors.



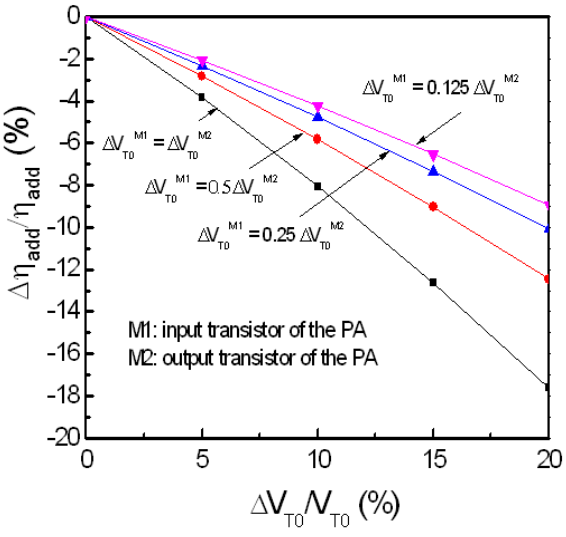
(a)



(b)

FIG. 9 NORMALIZED OUTPUT POWER VERSUS (A) THRESHOLD VOLTAGE AND (B) MOBILITY SHIFT

High drain current and high drain-source voltage result in large power dissipation, which causes device self-heating. The transistor temperature rise ΔT in M2 is generally larger than that in M1 due to larger dc current and ac power flowing through the output transistor M2. To account for a wide range of temperature rise, ΔT^{M1} = 1/8, ¼, ½, and $1\times\Delta T^{M2}$ are simulated. Both the output power and power-added efficiency decrease with increasing temperature resulting from device self-heating as shown in Fig. 11.



(a)

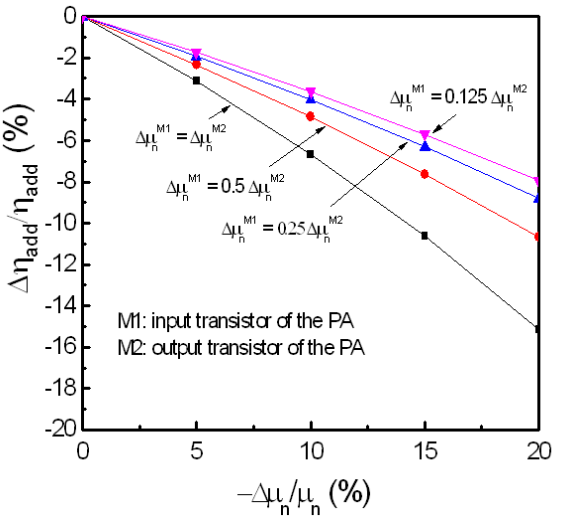


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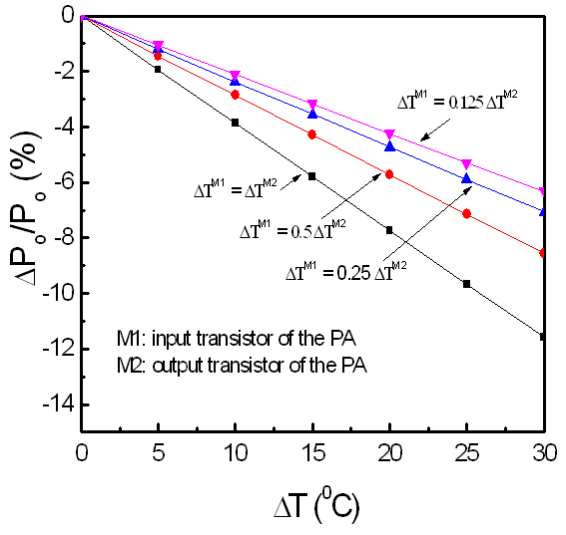
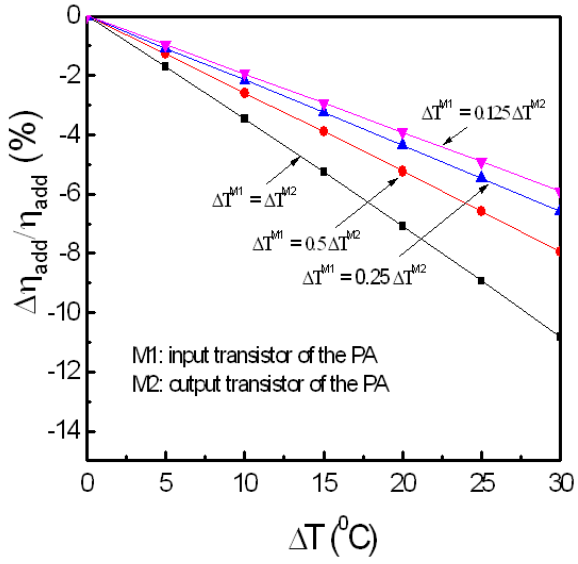
FIG. 10 NORMALIZED POWER-ADDED EFFICIENCY VERSUS (A) THRESHOLD VOLTAGE AND (B) MOBILITY SHIFT



(a)



(b)

FIG. 11 NORMALIZED (A) OUTPUT POWER AND (B) POWER-ADDED EFFICIENCY VERSUS TEMPERATURE RISE

Conclusion

A class F power amplifier at 5.8 GHz has been designed and analyzed. Its pre-layout and post-layout performances are compared. Post-layout parasitic effect decreases the output power and power-added efficiency. Physical insight of hot electron impact ionization and device self-heating has been examined using mixed-mode device and circuit simulation to mimic the class F PA operating environment. The output transistor has larger impact ionization rates and self-heating due to larger power dissipation and higher drain electric field than those of the input transistor. Hot electron effect increases the threshold voltage and decreases the electron mobility of the n-channel transistor, which in turn decreases the output power and power-added efficiency of the power amplifier, as evidenced by the RF circuit simulation results. The device self-heating also reduces the output power and power-added efficiency of the PA.

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